



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,090	07/31/2003	William B. Boyle	K35A1324	3202

35219 7590 10/19/2005

WESTERN DIGITAL TECHNOLOGIES, INC.
20511 LAKE FOREST DR. -C205
LAKE FOREST, CA 92630

EXAMINER

KO, DANIEL BOKMIN

ART UNIT PAPER NUMBER

2189

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/633,090	Applicant(s) BOYLE, WILLIAM B.	
	Examiner Daniel B. Ko	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |



DETAILED ACTION

This action is responsive to the application filed on 07/31/2003. Claims 1-16 have been submitted for examination.

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either on an application data sheet or supplemental oath or declaration.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2189

1. *Claims 1, 7, 9, and 15 rejected under 35 U.S.C. 102(b) as being anticipated by Chi et al. (US Patent Application 2002/0069351 A1).*

Regarding claims 1 and 9, Chi et al. teaches a disk drive control system comprising a micro-controller, a micro-controller cache system having a cache memory and a cache-control subsystem, and a buffer manager communicating with the micro-controller cache system and a remote memory, a method for improving fetch operations between the micro-controller and the remote memory via the buffer manager, the method comprising:

receiving a data-request from the micro-controller in the cache control subsystem wherein the data-request comprises a request for at least one of an instruction code and non-instruction data (page 4, paragraph 47; Chi et al. shows request for instruction);

providing the requested data to the micro-controller if the requested data reside in the cache memory (page 2, paragraph 15);

determining if the received data-request is for a non-instruction data if the requested data does not reside in the cache memory (page 3, paragraph 39; Chi et al. discloses the determining whether instruction is stored in the cache memory and it is inherent that non-instruction data does not reside in the cache memory);

fetching the non-instruction data from the remote memory by the micro-controller cache system via the buffer manager (page 3, paragraph 39; Chi et al. discloses instruction data fetching from the remote memory and it is inherent that non-instruction data can be fetched from the remote memory); and

bypassing the cache memory to preserve the contents of the cache memory and provide the fetched non-instruction data to the micro-controller (page 3, paragraph 37 and 39; Chi et al. discloses the cache memory for instruction and it is inherent that non-instruction data would not be stored in this cache memory and preserve the contents of the cache memory).

According to claims 1 and 7, if the requested data is non-instruction data and not reside in the cache then the non-instruction data should bypass the cache memory. How can a non-instruction data ever be stored to cache memory? Therefore, Applicant's claimed invention works like instruction cache.

Regarding claims 7 and 15, Chi et al. teaches a method, further comprising:
determining if the received data-request is for an instruction code if the requested data does not reside in the cache memory (page 3, paragraph 39); and
filling the cache memory if the received data-request is for an instruction code (page 3, paragraph 39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2189

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
2. *Claims 1-3, 7, 9-11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashiroya (US Patent 6,647,463 B2) and Liu et al. (US Patent 6,922,754 B2).*

Regarding claims 1 and 9, Yamashiroya teaches a disk drive control system comprising a micro-controller, a micro-controller cache system having a cache memory and a cache-control subsystem, and a buffer manager communicating with the micro-controller cache system and a remote memory, a method for improving fetch operations between the micro-controller and the remote memory via the buffer manager, the method comprising:

receiving a data-request from the micro-controller in the cache control subsystem wherein the data-request comprises a request for at least one of an instruction code and non-instruction data (column 5, lines 52-55);

providing the requested data to the micro-controller if the requested data reside in the cache memory (column 5, lines 64-67; column 6, lines 1-3);

Art Unit: 2189

determining if the received data-request is for a non-instruction data if the requested data does not reside in the cache memory (column 6, lines 4-12);

fetching the non-instruction data from the remote memory by the micro-controller cache system via the buffer manager (column 12, lines 18-38).

Yamashiroya fails to teach bypassing the cache memory and provide the fetched non-instruction data to the micro-controller.

Liu et al. teaches "bypassing the cache memory to preserve the contents of the cache memory and provide the fetched non-instruction data to the micro-controller" (column 1, lines 47-56; column 10, lines 23-35; Liu et al. discloses bypassing the cache memory based on many factors including type of data request and it is obvious non-instruction data may be the type of data for bypassing based on locality of reference).

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Yamashiroya with Liu et al. The motivation for doing so would have been an avoiding the latencies associated with cache. Liu et al. states that through intelligent management and caching of data flow, invention is able to avoid some of the latencies associated with cache (column 1, lines 49-52).

Regarding claims 2 and 10, Yamashiroya teaches a method, wherein the determining is based on a signal received from the micro-controller (column 7, lines 52-66).

Regarding claims 3 and 11, Yamashiroya teaches a method wherein the fetching further comprises:

transmitting a cache control subsystem data-request from the cache control subsystem to the buffer manager;

accessing the remote memory by the buffer manager; and

retrieving the cache control subsystem requested data from the remote memory (column 12, lines 18-38).

Regarding claims 7 and 15, Yamashiroya teaches a method, further comprising:

determining if the received data-request is for an instruction code if the requested data does not reside in the cache memory; and

filling the cache memory if the received data-request is for an instruction code (column 6, lines 4-12).

3. *Claims 4-6, 8, 12-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashiroya (US Patent 6,647,463 B2) and Liu et al. (US Patent 6,922,754 B2) and further in view of Henson et al. (US Patent Application 2002/0065994 A1).*

Regarding claims 4 and 12, Henson et al. teaches a method, wherein the buffer manager is in communication with a plurality of control system clients and provides client-requested data to the clients from the remote memory (page 1, paragraph 6).

Regarding claims 5 and 13, Henson et al. teaches a method, wherein the plurality of control system clients comprises at least one of a disk subsystem (page 2, paragraph 27), an error correction code subsystem (page 2, paragraph 29), and a host interface subsystem (page 3, paragraph 30).

Regarding claims 6 and 14, Henson et al. teaches a method, wherein the remote memory comprises a dynamic random access memory (DRAM) (page 1, paragraph 6).

Regarding claims 8 and 16, a burst fill of the cache memory is obvious feature and well known in the art.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Yamashiroya and Liu et al. with Henson et al. The motivation for doing so would have been an improving head tracking and seek performance. Henson al. states that through reducing the uncertainty delay in starting the head servo interrupt service routine, there is about 10 percent overhead reduction in running the routine, thereby improving head tracking and seek performance (page 2, paragraph 18).

Conclusion

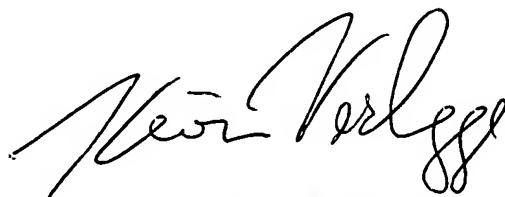
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel B. Ko
AU 2189



KEVIN VERBRUGGE
PRIMARY EXAMINER